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02-27-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: GURUPRASAD G. RAO ET AL.

COPY OF PAPERS
ORIGINALLY FILED

Filed: JULY 13, 2001

For: APPARATUS AND METHODS FOR CONSTRAINT
CHARACTERIZATION WITH DEGRADATION OPTIONS

Serial No.: 09/904,630

RECEIVED

Group Art Unit: 2123

FEB 05 2002

Examiner: UNKNOWN

Technology Center 2100

Atty Dkt: SIME:002

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in a first class, postage prepaid envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below:

12-20-01
Date

Marty Bauer
Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R. §§ 1.97(g),(h), this Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

The present Information Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in

accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/SIME:002.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



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Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.

SIME:002

Serial No.

09/904,630

Applicant

GURUPRASAD RAO ET AL.

Filing Date:

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2123

U.S. Patent Documents

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Foreign Patent Documents

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Other Art

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U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A1						

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C2	Daniel Auvergne et al., "Signal Transition Time Effect On CMOS Delay Evaluation," IEEE Transactions On Circuits and Systems-I: Fundamental Theory and Applications, Vol. 47, No. 9, September 2000, pps. 1362-1369.
	C3	Lindsay Kleeman et al., "Metastable Behavior In Digital Systems," IEEE Design and Test of Computers, December 1987, pps. 4-19.
	C4	Charles Dike, "A Metastability Primer," Signetics, Note AN219, November 1989, pps. 1-3.
	C5	Yusuf Leblebici, "Design Considerations For CMOS Digital Circuits With Improved Hot-Carrier Reliability," IEEE Journal Of Solid-State Circuits, Vol. 31, No. 7, July 1996, pps. 1014-1024.
	C6	Lee-Sup Kim et al., "Metastability of CMOS Latch/Flip-Flop," IEEE Journal of Solid-State Circuits, Vol. 25, No. 4, August 1990, pps. 942-950.
	C7	J. Juan-Chico et al., "CMOS Inverter Maximum Frequency Of Operation Due To Digital Signal Degradation," Electronics Letters, Vol. 33, No. 19, September 11, 1997, pps. 1619-1621.

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Examiner:

Date Considered:

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.